

PegaSim

High Performance, Mixed-Language Digital Logic Simulator

PegaSim is a high-performance and mixed-language digital logic simulator. PegaSim utilizes innovative algorithms to achieve a high-performance simulation and constrained random solver. It supports design and verification languages including SystemVerilog, Verilog, VHDL, and UVM methodology.

PegaSim works with Genesis modeling, OmniArk emulation, Prodigy FPGA prototyping, and Cloud Service to meet various verification needs. It accelerates SoC verification across multiple scenarios from IP and subsystem verification to full system validation.

Highlights

- Supports SystemVerilog, Verilog, and VHDL
- Supports UVM, VMM, and OVM methodologies
- Supports SDF and Timing Check
- Full DPI and VPI support
- Supports incremental and parallel compilation
- Competitive compilation and runtime performance



Features

► Comprehensive language support

- Verilog (IEEE 1364)
- SystemVerilog (IEEE 1800-2017)
 - Includes SVA assertions, constrained random solver, and functional coverage
 - Full DPI and VPI support
- UVM methodology (IEEE 1800.2)
 - Supports UVM, VMM and OVM methodologies
- VHDL (IEEE 1076-1993)
 - Supports std_logic_1164, numeric_std, etc.
 - Supports IP encryption (IEEE 1735)

► Cross-language (VHDL/SV) interoperability

- Can instantiate VHDL inside SV, or SV inside VHDL to arbitrary depth
- Instances can override parameters/generics
- Appropriate type conversions on port connections

► Code coverage

- Supports line/block, toggle, expression coverage analysis
- Supports assertion coverage analysis

► Multiple simulation techniques

- Incremental and parallel compilation
- SDF and Timing Check
- Co-simulation with emulation and FPGA prototyping

► High-performance & Mixed-language

- VHDL, Verilog & SystemVerilog mixed simulation
- Large-scale design simulation, such as hundreds of millions of gates
- Competitive compilation and runtime performance

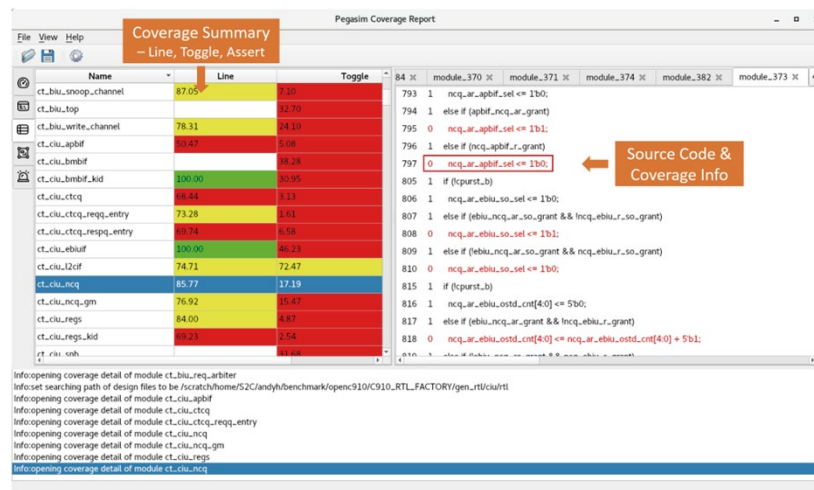
Features

► Easy to deploy and use

- Supports multiple processor architectures – X86, RISC-V, ARM
- Supports cloud deployment and parallel execution of regression tasks on the cloud
- Supports VCD and self-developed waveform formats for waveform analysis and source code debugging

Coverage Analysis

During chip validation, verification completeness is measured with RTL code coverage. PegaSim integrates the coverage analysis tool to support coverage-driven verification, coverage goal reports, and coverage hole detection.



Coverage Analysis Window

One-stop Shop for Your Verification Needs

As chip design integration and complexity grow, heterogeneous verification has become an important method for functional validation. The launch of PegaSim marks the completion of S2C's heterogeneous verification platform. This platform supports various verification scenarios for complex systems or chips, including IP/Modular simulation, emulation, and FPGA prototyping. Collectively, the comprehensive verification solution ensures that the entire chip design flow aligns with the required specifications and that the project works as the expected verification plan.

